#6 5/31/00 8/16

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Applicant: Chu et al.
Filed: January 28, 1999
For: DELAY-LOCKED-LOOP (DLL) HAVING SYMMETRICAL RISING AND FALLING..

Serial No.: 09/239,487
Group Art Unit: 2816
Examiner: D. Le
Atty Dkt No.: 99 P 7445 US
Date: May 23, 2000

CERTIFICATE OF MAILING
PURSUANT TO 37 CFR §1.8

I hereby certify that this correspondence is being deposited on **May 22, 2000** with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Assistant Commissioner for Patents
Washington DC 20231

Date of
Signature: May 22, 2000

Stanton C. Braden
Reg. No.: 32,556

Assistant Commissioner for Patents

Washington DC 20231

RESPONSE

Sir:

In response to the action mailed March 20, 2000, please amend the application as follows:

IN THE CLAIMS

1. (Amended) A circuit, comprising:

a receiver for receiving an input train of pulses; and

a delay-locked-loop coupled to an output of the receiver, the delay-locked-loop comprising:

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